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## Remarks

Applicant respectfully requests reconsideration of this application. Claims 1, 12, 68, 77, 104-106, 110-112, 116-118 and 122-124 have been amended to correct minor informalities and to more distinctly claim the presently invented subject matter. New claims 127-136 have been added to the application. No claims stand allowed.

### *Non-Art Rejections - 35 U.S.C. § 112*

Claims 107, 108, 113, 114, 119, 120, 125 and 126 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the examiner considers that support is not found in the original disclosure for a first conduction channel with a thickness of 0.5 to 1.0 microns and the buried layer thickness of 1.0 to 1.5 microns.

Figure 12 and the corresponding discussion on page 23, line 6 through page 24, line 4, of the specification clearly shows a buried layer region formed at a distance between about 1.0 and 2.0 microns below the substrate surface. For example, the plot of Figure 12 shows an upper JFET conduction channel and a buried layer region both having a thickness of about 1.0 um. The specification on page 24, lines 2-3 explicitly states that the buried region is only about 1.0 um wide. The discussion on page 24, lines 5-11 further indicates that the buried region may be formed between about 0.5 to 2.0 um (i.e., 1.5 um thick). Figure 13 shows another embodiment with an upper JFET conduction channel of about 0.5 um thick. Hence, it is respectfully submitted that Applicant's disclosure supports the claimed range of thicknesses.

Claims 104-106, 110-112, 116-118 and 122-124 also stand rejected under 35 U.S.C. § 112, second paragraph, as being considered indefinite with respect to the term "charge" recited in the claims. Applicant has amended these claims to more

distinctly claim the subject matter of the claimed invention by replacing "charge" with the term -- doped impurity --. Accordingly, it is respectfully submitted that all claims now fully satisfy the requirements of the statute.

### *Art Rejections - 35 U.S.C. § 103(a)*

Claims 1-4, 6-8, 10, 12-14, 17-19, 23, 58-78, 80-83 and 103-126 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams et al. (US 5,386,136; "Williams") in view of Yamanishi, et al. (JP404107877A; "Yamanishi"), or alternatively, obvious over Yamanishi in view of Williams. Additionally, claims 127 and 128 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rumennik et al. (US 5,258,636; "Rumennik") in view of Yamanishi. Applicant has amended independent claims 12, 68 and 77 to more distinctly claim and to further distinguish the present invention from the prior art.

Applicant respectfully submits that *prima facie* obviousness is absent because (1) there is no suggestion, teaching, or motivation to modify or combine the cited references so as to arrive at the claimed invention; (2) there is no reasonable expectation of success by the hypothetical person of ordinary skill in the art at the time the invention was made that the proposed combination or modification would work to produce beneficial results; and (3) the prior art fails to teach or suggest all of the elements and limitations recited in the claims.

As the attached Rule 1.132 declaration attests, a person of ordinary skill following the teachings would have lacked any reasonable expectation of success of attaining Applicant's invention since Yamanishi's dopant desegregation processing technique was known to be highly unpredictable and very difficult to control. The declaration further attests to the fact that Yamanishi's device is inoperative to provide a HVFET device with first and second extended drain conduction channels.

With respect to amended claims 12, 68, 77 and newly added claim 127, a person of ordinary skill would certainly have lacked any expectation of success in

attaining an HVFET with "a first conduction channel having a doped impurity concentration of approximately 1 X $10^{12}/cm^2$ or greater". Neither Yamanishi nor Williams teach, disclose or suggest a HVFET with "a first conduction channel having a doped impurity concentration of approximately 1 X $10^{12}/cm^2$ or greater" as recited, for example, in amended claim 1. Indeed, Yamanishi is completely silent as to the doped impurity concentration in his N-type construction at the surface of the substrate.

The existence of first and second conduction channels is not inherent in Yamanishi's device structure. A retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination. An allegedly inherent characteristic must *necessarily* flow from the teachings of the applied prior art. In this case, there is no teaching in Yamanishi (or the other cited prior art) that reasonably supports the conclusion that his device structure necessarily includes first and second conduction channels – much less with the first conduction channel having a doped impurity concentration of approximately 1 X $10^{12}/cm^2$ or greater.

In this case, there is no logical reason apparent from the cited prior art references for a person of ordinary skill in the art to achieve first and second conduction channels in an extended drain structure in order to improve the operating characteristics of a high voltage field-effect transistor. As explained above, a reasonable expectation of success does not exist in the prior art; therefore, while it may have been obvious ***to try***, it would not have been obvious ***to do***. Obviousness cannot be predicated upon what a person skilled in the art might find obvious to try, but only on what the prior art would have led a person skilled in the art to do.

Accordingly, Applicant respectfully requests that the rejection of claims 1-4, 6-8, 10, 12-14, 17-19, 23, 58-78, 80-83 and 103-128 under 35 U.S.C. § 103(a) be withdrawn.

It is respectfully submitted that all claims are now in condition for allowance.

Please charge any shortages and credit any overcharges to our Deposit Account No. 50-2060.

Respectfully submitted,

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agreed to the changes.

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Caitlin Burgess — September 6, 2002 Date

## Versions with Markings to Show Changes Made

12. (Amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed within the substrate;

a source diffusion region disposed in the substrate spaced-apart from the first region, an IGFET channel region being formed between the source diffusion region and the first region;

a drain diffusion region disposed in the first region;

a buried region of said first conductivity type disposed within the first region, the buried region forming JFET channels within the first region, one JFET channel being formed above the buried region with a doped impurity concentration of 1 X $10^{12}/cm^2$ or greater and another JFET channel below the buried region, the buried region being spaced-apart from the drain diffusion region;

an insulated gate formed above the IGFET channel region.

68. (Amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having a laterally extended portion that forms a lateral boundary with the substrate;

a drain diffusion region of the second conductivity type disposed in the first region and separated from the lateral boundary by the laterally extended portion;

a second region of the first conductivity type disposed in the substrate;

a source diffusion region of the second conductivity type disposed in the second region, a channel region being formed between the source diffusion region and the lateral boundary;

an insulated gate disposed above the channel region;

a buried region of the first conductivity type sandwiched within the laterally extended portion of the first region to form a junction field-effect device in which current flows in the first region both above and below the buried region, a doped impurity concentration in the first region above the buried region being about 1 X $10^{12}/cm^2$ or greater.

77. (Amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having a laterally extended portion that forms a lateral boundary with the substrate;

a drain diffusion region of the second conductivity type disposed in the first region and separated from the lateral boundary by the laterally extended portion;

a source diffusion region of the second conductivity type disposed in the substrate and spaced-apart from the lateral boundary of the first region, a channel region being formed between the source diffusion region and the lateral boundary;

an insulated gate disposed above the channel region;

a first buried layer of the first conductivity type disposed in the substrate beneath the source diffusion region;

a second buried layer of the first conductivity type sandwiched within the laterally extended portion of the first region and spaced-apart from the lateral boundary so as to act as an effective gate controlling dual current channels in the first region both above and below the second buried layer, a doped impurity concentration in the first region above the second buried region being about 1 X $10^{12}/cm^2$ or greater.

104. (Amended) The HVFET according to claim 1 wherein the buried region has a [charge] doped impurity concentration approximately twice that of the first conduction channel.

105. (Amended) The HVFET according to claim 1 wherein the buried region has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

106. (Amended) The HVFET according to claim 1 wherein the second conduction channel has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

110. (Amended) The HVFET according to claim 12 wherein the buried region has a [charge] doped impurity concentration approximately twice that of the one JFET channel.

111. (Amended) The HVFET according to claim 12 wherein the buried region has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

112. (Amended) The HVFET according to claim 12 wherein the another JFET channel has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

116. (Amended) The HVFET according to claim 68 wherein the buried region has a [charge] doped impurity concentration approximately twice that of the first region above the buried layer.

117. (Amended) The HVFET according to claim 68 wherein the buried region has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

118. (Amended) The HVFET according to claim 68 wherein the first region below the buried layer has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

122. (Amended) The HVFET according to claim 77 wherein the second buried region has a [charge] doped impurity concentration approximately twice that of the first region above the second buried layer.

123. (Amended) The HVFET according to claim 77 wherein the second buried region has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.

124. (Amended) The HVFET according to claim 77 wherein the first region below the second buried layer has a [charge] doped impurity concentration of approximately 2 X $10^{12}/cm^2$.